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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,059	06/24/2003	Charles N. Perez	BUR920030032US1	1058

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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,059	PEREZ ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06/24/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *7-12 and 18-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5;13-17; and 25-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/24/03*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20050615*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-5; 13-17; and 25-29 (Group I), drawn to a method displaying a guard ring, classified in class 716, subclass 11.

   II. Claims 6-12 and 18-24 (Group II), drawn to a method design a guard ring, classified in class 438, subclass 140.

2. Inventions Group I and Group II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because Group I is combination of a method displaying and incorporating a guard ring of integrated circuit. It does not need to verify aspects. The subcombination has separate utility such as Group II, a method incorporating a guard ring of integrated circuit. It does not need a display unit.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with the Applicant's attorney Mr. Richard Kotulak (Reg. No. 27712) on June 16, 2005 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-5, 13-17 and 25-29. Affirmation

of this election must be made by applicant in replying to this Office action. Group II, claims 6-12 and 18-24 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention. The Applicant's are requested to cancel claims 6-12 and 18-24 in the next office communication.

Specification

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: " Method of displaying a Guard Ring within an integrated circuit".

Claim Objections

6. Claim 1 is objected to because of the following informalities: claim 1, line 8, the term "and" before "symbolically", should rewrite in "or". Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-5, 13- 17, and 25-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salling et al. (Salling) (US 2004/0114287) in view of Kishida et al. (Kishida) (US 2001/0053948).

9. **With respect to claims 1 and 25**, Salling disclose a method of displaying (appearing) a guard ring within an integrated circuit design having a logic design (fig. 1,

elements 110, 120). As figure 1, guard rings 110 and 120 are forming (incorporating) into an integrated circuit design. Such as, guard ring (110) in the substrate (106), which is surrounding the discharge circuitry (101) and drive circuitry (102) and the guard ring (120) in substrate (106), which is surrounding the guard ring (110) and connect to VSS/ ground potential.

Salling also disclose a graphically display logic device and guard ring in a single display (appear electrically " floating") (fig. 1, 2 and 3; pg. 3. ¶ 32, ll.1-6), and keeping an equal distance position and various geometrical shape of both guard rings and logic device in an integrated circuit (pg. 3. ¶ 32; pg. 4, ¶ 42, ll. 5-6). However, Salling does not explicitly show a means to display the design with a guard ring.

(claim 25) Salling does not disclose a program storage device readable machine, tangibly embodying a program of instructions executable by the machine to perform a displaying a guard ring within an integrated circuit.

Kishida explain more specifically about the relationship position among logic device in arrange a layout cell (Kishida, pg. 4, ¶ 69, ll. 4-7), which is displaying a guard ring in circuit layout (Kishida, fig. 7, guard ring (88), pg. 3, ¶ 61, ll. 1-8).

Furthermore, Kishida disclose a program storage device readable machine, tangibly embodying a program of instructions executable by the machine to perform a displaying a guard ring within an integrated circuit (Kishida, fig. 1, 2, 4, and 5; page 1, ¶ 4-6).

It would have been obvious to a person of ordinary skill in the art at the time of Applicant's invention to reference and combine the teachings of Kishida with Salling for editing a circuit layout more efficient (Kishida, pg. 2, ¶ 32, ll. 1-4), then guard ring can

easily be adopted into any integrated circuit design methodology (Salling, pg. 2, ¶ 14, ll. 2-3). However, Kishida using automatic tools and programming for displaying the circuit layout on the layout window, that would help the user determines whether there is any additional layout cell to be displayed or any layout editing to be redone (Kishida, pg. 1, ¶ 10).

10. **With respect to claim 13**, Salling disclose a method of displaying at least one guard ring within a hierarchical integrated circuit design having logic devices (Salling, fig. 3, first guard ring 110, second guard ring 120, and third guard ring 310), said method comprising:

incorporating said guard ring into said portion of said hierarchical integrated circuit design (fig. 1, element 110, 120, and 310); and

displaying said portion of said integrated circuit design as a cell having a guard ring within said hierarchical integrated circuit design (appear electrically " floating") (fig. 1, 2 and 3; pg. 3. ¶ 32, ll.1-6).

Salling teach position between the guard rings (pg. 3. ¶ 32), and also mention about relative position between logic device and guard ring (pg. 3, ¶ 34, ll. 6-9), but Salling do not solid clarify the relative position between logic device and guard ring.

Kishida explain more specifically about the relationship position among logic device in arrange a layout cell (Kishida, pg. 4, ¶ 69, ll. 4-7), which is displaying a guard ring in circuit layout (Kishida, fig. 7, guard ring (88), pg. 3, ¶ 61, ll. 1-8).

It would have been obvious to a person of ordinary skill in the art at the time of Applicant's invention to reference and combine the teachings of Kishida with Salling for editing a circuit layout more efficient (Kishida, pg. 2, ¶ 32, ll. 1-4), then guard ring can easily be adopted into any integrated circuit design (Salling, pg. 2, ¶ 14, ll. 2-3). However, Kishida using automatic tools and programming for displaying the circuit layout on the layout window, that would help the user determines whether there is any additional layout cell to be displayed or any layout editing to be redone (Kishida, pg. 1, ¶ 10) or additional another hierarchical (level) of guard ring without departing from the spirit and scope (Salling, pg. 4, ¶ 44, ll.2-4).

11. **With respect to claims 2-4, 14-16, and 26-28**, Salling and Kishida disclose all the limitations in claims 1, 13, and 25.

Salling and Kishida further disclose a displaying parameter symbol including the type of circuit (Salling, pg. 4, claim 7); type of guard ring (Salling, pg. 4, ¶ 40, ll. 16-19; ¶ 42, ll. 1-3; and ¶ 43, ll.1-9); and the efficiency of guard ring (Salling, pg. 4, ¶ 42, ll. 5-6, claim 4, and claim 6).

12. **With respect to claims 5, 17, and 29**, Salling and Kishida disclose all the limitations in claims 1 and 25.

Salling and Kishida also further disclose a guard ring graphically comprise illustrating relative position of said logic device and guard ring (Salling, pg. 3, ¶ 34, ll. 6-9, ¶ 32, ll. 3-8).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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